Apoorva Sinha

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Professional Summary

Computer Science graduate student specializing in AI and Machine Learning at Georgia Institute of Technology.Prior experience in the electronics industry as an analog engineer at Texas Instruments.Enhanced the analytical background in AI/ML technologies through academic projects and research. Seeking a SW/ML Engineering role to contribute to impactful projects and develop innovative solutions starting June 2025.

Education

Georgia Institute of Technology — Atlanta, GA
*MS in Computer Science (**GPA: 4.0/4.0**)* — *Expected May 2025*

Indian Institute of Technology Kharagpur — Kharagpur, India
*Dual Degree (B.Tech + M.Tech) in Electrical Engineering and Control Systems Engg. (**CGPA: 8.75/10.0**)* — *May 2018*

Technical Skills

Programming Languages: Python, C, C++,Rust,Java,Javascript
AI/ML Frameworks: TensorFlow, PyTorch, scikit-learn
Data Analysis Tools: Pandas, NumPy, R,d3.js,Tableau
Tools & Technologies: Git, GitHub, MATLAB, GDB, Valgrind,Docker
Databases: MySQL,PostreSQL,SQLite
Relevant Coursework:Advanced Operating Systems,Distributed Computing,Advanced Computer Networks, Introduction to Graduate Algorithms,Design and Analysis of Algorithms, Machine Learning, Deep Learning, Artificial Intelligence, Computer Vision,Data and Visual Analytics

Experience

Graduate Teaching Assistant — May 2024 – Present
Georgia Institute of Technology — *Atlanta, GA*

- Assist in teaching **CS8803/CS7400: Introduction to Quantum Computing** to over 120 students across Summer and Fall semesters.
- Collaborate with faculty to develop course materials and enhance curriculum related to quantum algorithms and computational models.
- Provide guidance on programming assignments, fostering student understanding of complex quantum computing concepts.

Summer Research — May 2024 – Present
Georgia Institute of Technology — *Atlanta, GA*

- Worked on analysis and development of Defect Tolerant Quantum LDPC codes
- Developed methods to repair quantum error-correcting codes for **QLDPC** codes, contributing to advancements in quantum computing error mitigation, especially for IBM's Gross Code $[[144, 12, 12]]$
- Implemented a modified **Belief Propagation-OSD** algorithm in **Python** and **C**.
- Collaborated with a team to test and validate the code, ensuring reliability and scalability of solutions.

Analog Electronics Engineer — June 2018 – May 2021
Texas Instruments Inc. — *Bangalore, India*

- **Product & Validation Engineer**: Spearheaded characterization, validation, and statistical analyses for mixed-signal silicon isolation chips, contributing to the tapeout of 12 device families for several isolated LVDS,CAN,RS-485 and USB devices.As the bench engineer designed the validation automations using LabVIEW and Python for Cross Temperature characterization.
- **Embedded Firmware Designer**: Developed low-level firmware interfaces in **C** and **C++** for embedded systems, accelerating HW(RTL)-SW co-development cycles by 600%.
- **RF Circuit Designer**: Designed high-frequency circuit blocks for mixed-signal chips supporting **USB 2.0** for the isolated device families ISOUSB111/ISOUSB211, enhancing signal integrity and reducing power consumption.
- Collaborated with cross-functional teams to define requirements and deliver robust hardware and software solutions.
- Led testing and debugging efforts, utilizing tools to proactively address issues and ensure system reliability.

Research Assistant — May 2017 – Aug 2017
University of Winnipeg (MITACS Fellowship) — *Manitoba, Canada*

- Conducted theoretical research on thermodynamic properties in String Theory, applying computational techniques to model non-equilibrium behavior.
- Developed **Python** scripts to simulate the evolution of string distributions using the numerical Boltzmann transport equations.

Analog Engineering Intern May 2016 – July 2016
Texas Instruments Inc. *Bangalore, India*

- Implemented jitter measurement algorithms for high-speed data links
- Created a software suite for jitter analysis using **C++**, **Python**, and **MATLAB**, integrating with multiple instruments via GPIB protocol.

Projects

Bus Bunching Detection and Mitigation | ***Python,Javascript*** January 2025 – April 2025

- Developed and trained a **RL agent** to mitigate bus bunching based on historical traffic data from **New York** and **Atlanta** using **Python**
- Developed an **Early Warning System** for potential buses/roads that might be congested using **Machine Learning** achieving a **92 %** precision using **Ensemble models**.
- Developed a dashboard using **express.js** for live tracking of buses on **New York** and **Atlanta** maps.Deployed the trained ML model for live prediction of potential bunching scenarios. Backend using **node.js**.

GT Store Distributed Key-Value Store | ***C++, gRPC, Consistent Hashing*** November 2024 – December 2024

- Designed and implemented a distributed key-value store with a lightweight centralized manager and multiple storage nodes; offloaded data partitioning and load balancing to clients via consistent hashing.
- Developed gRPC-based RPC interfaces for node registration, heartbeat, put/get operations, and dynamic retrieval of active storage nodes.
- Built client-side replication (configurable factor) and versioning to guarantee strong write consistency and eventual read consistency under node failures.
- Instrumented heartbeat monitoring and failure detection in the manager, automatically removing inactive nodes and enabling predecessor takeover of key ranges.
- Executed performance benchmarks on an MacOS and Unix machine, analyzing throughput impact of replica count and load-balance histograms to identify non-uniform hash distributions.

Defect Mitigation in Bivariate Bicycle QLDPC Codes | ***Python*** May 2024 -August 2024

- Surveyed superconducting quantum processor architectures and identified limitations of planar surface codes under fabrication defects.
- Analyzed Bivariate Bicycle (BB) Quantum Low Density Parity Check Codes(QLDPC) codes' non-planar connectivity and space-efficiency advantages over surface codes, leveraging 3D routing via Through-Silicon-Vias.
- Developed super-check construction strategies for BB codes: combined three broken X/Z checks per data-qubit defect into multiple valid superchecks, extending surface-code defect techniques.
- Characterized defect impacts on code distance and syndrome extraction; proposed modified extraction circuits to accommodate repaired connectivity.
- Performed circuit-level and code-capacity simulations to evaluate repair strategies on the $[[144, 12, 12]]$ Gross code, demonstrating resilience to up to two simultaneous qubit or check failures.

Battery Management System using Deep Learning | ***Python, PyTorch*** January 2024 – April 2024

- Re-implemented and extended Nascimento et al.'s hybrid physics–data RNN in PyTorch, combining reduced-order electrochemical models with MLP-based non-ideal voltage estimation to predict **State of Charge**(SOC) and **State of Health**(SOH).
- Designed a two-stage training pipeline: (1) joint training of MLP non-ideal voltage networks across 12 NASA 18650 LCO battery cycles; (2) per-battery calibration of internal resistance R_0 and capacity q_{max}, achieving 35 mV worst-case SOC error (1.1 %).
- Demonstrated strong generalization: physics-informed model trained on constant-current discharges predicted random-walk load voltage with 22.9 mV (0.7 %) error and 7.8 % drift over 20 h.
- Explored PINN-GRU architecture embedding physics constraints into loss, analyzed convergence dynamics, and identified trade-offs between model complexity and training stability.
- Conducted extensive hyperparameter studies (loss functions, optimizers, learning rates) and performance benchmarks on M1 MacBook and Dell Precision, reducing training time by 70% via frozen-MLP calibration.